REMARKS

Status of the Claims

In the Office Action, claims 1-28 were noted as pending in the application. All claims stand rejected.

A. Rejection of Claims 11-15, 17, 20-24 and 26 under 35 U.S.C. § 103(a).

On page 7 of the Office Action, claims 11-15, 17, 20-24 and 26 were rejected under 35 U.S.C. § 103 as being obvious over U.S. Patent Application Number US 2002/0088003 to Salee, ("Salee") in view of U.S. Patent Number 6,698,022 to Wu ("Wu"). The reasons that the claims patentably distinguish over the reference are addressed below.

B. Summary of Cited References

Before addressing the Examiner's rejections, a brief summary of the cited references is provided.

Salee

Salee relates to a system for providing redundancy in a data over cable network that includes a plurality of CMTSs. ¶ 2. A timer preset register in a master CMTS stores a preset value and a comparator initiates a SyncPulse signal to slave CMTSs when a timer value equals the value stored in the present register. ¶ 13. The timer preset value in every CMTS – including the master and all slaves - is set to the same value. ¶ 14 When the comparator of the master CMTS indicates a match between the preset register and the timer counter of the master, the SyncPulse signal then goes out to the slave CMTSs and instructs each salve to load the value from its respective preset register into its timer counter. *Id.*, ¶ 15, Claim 3. Thus, the timer counters of all CMTSs are synchronized at a frequency that is based on the value in the preset registers. ¶ 15. Changing the preset value P changes the time between SyncPulses being sent from the master to slave CMTSs. *Id.*

Wu

Wu relates to "recovering a global timing reference from a plurality of timestamps periodically transmitted from [a] CMTS." Col. 3, lines 60-62. To avoid using a relatively costly VCO, adjusts the local clock counter of a cable modem instead of adjusting the counter frequency. Col. 4, lines 48-50. To correct for jitter, clock drift and cable delays, a software interrupt is used to adjust the local timer clock value according to a mathematical algorithm that computes adjustment values based on timestamps received from a CMTS. Col. 6, lines 39-44. Thus, if modeling parameters are chosen correctly, the mathematical equation/algorithm can use received timestamp values and local clock values to estimate a jitter-free timestamp value T_c for every local clock counter t. Col. 5, lines 52-53.

C. The Claims are not Obvious over the Cited References

Applicant respectfully submits that the subject matter of the claims patentably distinguish over the cited references. Under MPEP § 2142, for an examiner to establish a *prima facie* case of obviousness, "three basic criteria must be met. First, there must be

some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure." If any of these three criteria are not met, the Examiner has not met the burden of establishing a *prima facie* case of obviousness, and the rejection should be withdrawn.

Furthermore, each dependent claim includes all of the limitations of the independent claim from which it depends. If an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is non-obvious. MPEP §2143.03, citing In re Fine, 837 F.2d 1071 (Fed. Cir. 1988). Applicant respectfully submits that the burden of establishing a *prima facie* case of obviousness has not been met.

D. Claims are not obvious over the cited references

Regarding independent claims 11 and 20, a first value of a timing counter of a first circuit card is copied to a storage device, an offset is added to this value to create a future timing value that is then copied into the timing counter of a second circuit card. Claims 15 and 24 claim system hardware for facilitating the methods of claim 11 and 20. A timing value is written periodically from a system controller master to a circuit card slave. Page 14, lines 9-12. To obviate error caused by delay in writing the timing value from the master to the slave, a predetermined offset is added to the value of the master timing value before it is stored to the timing counter of the spare card. Page 14, lines 19-21. "The increased count value should be created such that the actual loading of this increased count value into the slave timing counters (after distribution from the system Controller card to the cable interface cards) will occur exactly when the master timing counter on the system Controller card arrives at the value which is equal to the increased value." Page 15, lines 7-11. This provides the advantage that when a spare circuit card takes over for a failed circuit card, the timestamps are sent out from the newly-placed-into-service spare card in continuity with the timestamp stream that had been provided by the previous circuit card that the spare replaced. Page 15, lines 11-12.

This procedure is helpful when, for example, a circuit fails and a spare is automatically swapped into service as a replacement for the failed card. Or, when a card is physically replaced with a new card, and the new card takes over for a currently active card - a previously spare card, for example. In the latter case, the new card might have an empty timing counter register - capable of storing a timing value - because it has been out of service (i.e., on a shelf in a warehouse, for example), and would thus need a value placed into its timing counter. When a current timing counter value is distributed from the System Controller, by the time the value reaches the slave circuit cards, a finite amount of time will have passed, and the value will be stale, inasmuch as it represents a time that is not contemporaneous with the actual current time of the System Controller. By determining the amount of delay that occurs in distributing the timing value from the System Controller to the individual circuit cards, compensation is provided by adding this delay amount to the timing value from the System Controller, and then writing the sum to a given circuit card. Then, timestamps transmitted to the newly-placed-into-service card

are time-continuous with the stream of timestamps that a previous card had been transmitting.

The references, either alone, or in combination, do not disclose all of these claim elements, nor do they include a suggestion that the inventions disclosed collectively therein could be modified to result in the subject matter claimed in the remaining independent claims of the present application. Referencing paragraphs 13 and 14 of the office action, Examiner asserts that Salee discloses copying a future timing counter value from a storage device to a timing counter of a second device. However, as discussed above, at some point in time Salee initializes all slave cards with a value P.

This is not a future timing value. Rather, it is an arbitrary value with a dual role: determining how often a trigger signal is sent to each of a plurality of slave cards, and the value (P) that is loaded into the timer upon receiving said trigger signal. As discussed in Salee, the purpose is to alleviate the effects of timer drift. However, the initializing of the value P into each card is not discussed in Salee. Although Salee discusses that "[t]he contents of register 26 can . . . be controlled by the processor to vary the preset . . .", ¶ 14, lines 35-36, as highlighted by Examiner, the fact remains that slaves and the master are all reset with the same value P when the timer T of the master equals P. ¶ 14, lines 32-34. Thus, because the SyncPulse signal is sent to all slaves when T = P at the master, and because the value P is loaded into each of the slave timers when a SyncPulse signal is received, the timer value T of every slave is set to the same value P at the same moment in time. ¶ 14, lines 26-30. This would be a present timing counter value rather than a future timing counter value.

This contrasts with claims 11, 15, 20 and 24. The future timing counter value is derived to compensate for the delay in loading a value from the System Controller to each of the circuit cards, either active or spare. Since Salee discloses using a global SyncPulse signal to adjust a timer to a value already loaded on a given card, there is no need to load a future value timing value onto a circuit card because the value P already resides on the card. In contrast, in the present application, a finite amount of time elapses while a timestamp value is sampled from a first card, stored to a storage device, distributed to a circuit card, stored to a storage device and then used to initialize the timer of that card. It will be appreciated that it would be impossible to sample a timer value of a first card, store it, distribute it, receive it and use it to initialize a timer at a second card such that the timer of the second card and first card are the same value at any given time thereafter.

Thus, knowing the amount of time that elapses in performing the sampling, storing, distributing, receiving and initializing as discussed above, the use of the future timing counter value provides the benefit that the actual value used to initialize the second timer is a value that is the sampled value plus the expected time that will elapse while these steps are performed. Accordingly, the second timer is initialized at a given point in time with a value that is the same value that the sampled timer will have attained by that same given point in time. Since Salee initializes the slave cards with a value P at a frequency based on P (T and P are count numbers where the count increments at a rate based on the clock frequency) there is no disclosure of copying a future timing counter value into a storage device, nor of copying said future timing count value from said storage device into said timing counter of a second circuit.

Not only is a future timing counter value and the use thereof not disclosed in Salee, but Wu does not disclose sampling and copying a first timing counter value into a storage device and adding an offset to create a future timing counter value. As discussed above, Wu discusses using a software interrupt to adjust the local timer clock value according to a mathematical algorithm that computes adjustment values based on timestamps received from a CMTS to compensate for jitter, clock drift and cable delays. Similar to Salee (except Salee apprears to be directed toward synchronizing collocated CMTS devices whereas Wu relates to synchronizing a cable modem clock circuit with a remotely located CMTS clock.), Wu seeks to compensate for jitter and drift of a clock circuit at the cable modem. Col. 4, lines 35-36. Rather than adjusting the clock frequency so that it is the same as the clock frequency of the CMTS, Wu discusses adjusting the local clock counter. Col. 4, lines 45-50. While Wu discusses adjusting a timing counter count value to estimate the corresponding timestamp received from the CMTS, it does so based on values derived from a mathematical equation. Col. 5, lines 35-53. Modeling parameters, derived from a timestamp received from the CMTS and current local clock count values, are used to determine first and second adjustment values C_1 and C_2. Depending on the sign of C_1, C_2 may decrement or increment the second local clock counter, depending upon whether C_1 is positive or negative, respectively. Col. 7, lines 29-34. The adjustment of the second local clock counter is applied, along with the ranging offset, to synchronize the second local clock to the CMTS master clock. Col. 8, lines, 8-11. Thus, Wu is primarily concerned with adjusting for drift and jitter discrepancies between the local counter at the cable modem and the counter at the CMTS. While a ranging offset is also used, this offset, known in the art, is used to adjust for the propagation delay inherent in signals traveling the distance between a CMTS and a cable modem located at a user's location.

The future timing counter value "compensate[s] for the time required to transfer the new increased value into a local register 503 from which it can be clocked under the System Controller 502 into the local timing counter 512." Thus, because Wu discusses using a mathematical formula to estimate a time stamp based on a dynamic value, and the results of the mathematical formula can result in decrementing the local timing counter, as drift can manifest as an advance or delay, calculating a future timing counter value based on the time it takes to process the initializing of a new circuit is not disclosed in Wu.

Regarding the claim terms, the future timing counter value is defined in the specification of the present invention. Such limitations are included in the term as recited in the claims, and interpreting the claims to include this definition of the phrase future timing counter value does not require reading limitation into the claims that contain this phrase. Accordingly, because neither Salee nor Wu disclose calculating and using a future timing counter value to synchronize a plurality of CMTS circuits, or contain a suggestion to combine the references such that one skilled in the art would think of using a future timing counter value, the claims containing the language future timing counter value are not obvious over Salee in view of Wu. Accordingly, withdrawal of the rejection of claims 11, 15, 20 and 24 is respectfully requested.

Furthermore, since these claims are independent claims, all of the dependent claims that depend respectively therefrom are also not obvious. Therefore, withdrawal of the rejection of claims 12-14, 16-19, 21-23 and 25-28 is also respectfully requested under

MPEP §§2142 §2143.03, as these dependent claims also patentably distinguish over the references.

SUMMARY

For all the reasons advanced above, Applicant respectfully submits that the application is in condition for allowance and that action is earnestly solicited.

If the Examiner believes that there are any issues that can be resolved by a telephone conference, or that there are any informalities that can be corrected by an Examiner's amendment please contact the undersigned at the mailing address, telephone, facsimile number, or e-mail address indicated below.

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